WHAT IS CLAIMED IS:

1. A method for measuring the response of a voltage controlled oscillator within a phase locked loop comprising the steps of:

a) setting a voltage output of an integrator near a threshold voltage of a comparator;

b) holding a time period between a start of scan pulse and an end of scan pulse constant;

c) setting a digital to analog converter output voltage to its minimum value;

d) adjusting a counter M until said comparator equals said threshold voltage,

e) setting the digital to analog converter output voltage to another output voltage;

f) repeating steps (d) through (e) for as many intervals to meet precision requirements, and

g) returning said counter M to its nominal value which returns said voltage output of said integrator near said threshold voltage of said comparator.

2. The method according to claim 1, further comprising:

repeating steps d through e nine for an interval of nine times.

3. The method according to claim 1, further comprising the step of:

tabulating said M values against said digital to analog values.

4. The method according to claim 3, further comprising the step of:

Calculating an exact frequency for any voltage output of said digital to analog output.

5. The method according to claim 2, further comprising the step of:

providing a voltage output required by said digital to analog comparator when an instantaneous frequency is requested by the phase lock loop circuit by use of interpolation to create a requested frequency curve.

6. A phase locked loop circuit comprising:

an integrator having a voltage set near a threshold voltage of a comparator;

a digital to analog converter output set to a minimum value;

a counter M continuously adjusted until said comparator equals said threshold voltage, wherein said digital to analog converter output voltage is changed in stepwise fashion to another output voltage in association with said counter M for as many intervals needed to meet precision requirements

7. A phase lock loop circuit according to claim 6, further comprising:

said counter M returned to its nominal value which returns said voltage output of said integrator near said threshold voltage of said comparator.

8. A phase lock loop circuit according to claim 6, further comprising:

said digital to analog converter changed nine times.

9. A phase lock loop circuit according to claim 6, further comprising:

said M values tabulated against said digital to analog values.

10. The phase lock loop circuit according to claim 6, further comprising:

an exact frequency calculated for any voltage output of said digital to analog output.

11. The phase lock loop circuit according to claim 2, further comprising:

a requested frequency curve created by interpolation when said voltage output is required by said digital to analog comparator when an instantaneous frequency is requested by the phase lock loop circuit.

12. A phase locked loop system comprising the steps of:

means for setting a voltage output of an integrator near a threshold voltage of a comparator;

means for holding a time period between a start of scan pulse and an end of scan pulse constant;

means for setting a digital to analog converter output voltage to its minimum value;

means for adjusting a counter M until said comparator equals said threshold voltage;

means for setting the digital to analog converter output voltage to another output voltage wherein said means for adjusting and setting are repeated for as many intervals as necessary to meet precision requirements;

returning said counter M to its nominal value which returns said voltage output of said integrator near said threshold voltage of said comparator; and

calculating an exact frequency for any voltage output of said digital to analog output.

13. The phase lock loop system according to claim 12, further comprising:

means for tabulating said M values against said digital to analog values.

14. The phase lock loop system according to claim 12, further comprising:

means for providing a voltage output required by said digital to analog comparator when an instantaneous frequency is requested by the phase lock loop circuit by use of interpolation to create a requested frequency curve.